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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 10/533,751 | 05/04/2005 | Carsten Deppe | DE 020246 | 6706 |

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| EXAMINER | |
|---|---|
| FUTEL, GAYLA S | |
| **ART UNIT** | **PAPER NUMBER** |
| 2609 | |

| SHORTENED STATUTORY PERIOD OF RESPONSE | MAIL DATE | DELIVERY MODE |
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| 3 MONTHS | 03/22/2007 | PAPER |

**Please find below and/or attached an Office communication concerning this application or proceeding.**

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/533,751 | DEPPE ET AL. | |
| | Examiner | Art Unit | |
| | Gayla Futel | 2609 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) 1-11 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-11 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 05/04/2005 is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

## DETAILED ACTION

### *Drawings*

1. The drawings are objected to because more descriptive labels are needed for the boxes in Figures 1 and 3. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the examiner does not accept the changes, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

2. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the additional, activatable clock generator of a higher frequency must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the examiner does not accept the changes, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

***Specification***

3. Receipt is acknowledged of a certified copy of the DE102518068 application referred to in the oath or declaration or in an application data sheet. If this copy is being filed to obtain the benefits of the foreign filing date under 35 U.S.C. 119(a)-(d), applicant should also file a claim for such priority as required by 35 U.S.C. 119(b). If the application being examined is an original application filed under 35 U.S.C. 111(a) (other than a design application) on or after November 29, 2000, the claim for priority must be

presented during the pendency of the application, and within the later of four months from the actual filing date of the application or sixteen months from the filing date of the prior foreign application. See 37 CFR 1.55(a)(1)(i). If the application being examined has entered the national stage from an international application filed on or after November 29, 2000, after compliance with 35 U.S.C. 371, the claim for priority must be made during the pendency of the application and within the time limit set forth in the PCT and Regulations of the PCT. See 37 CFR 1.55(a)(1)(ii). Any claim for priority under 35 U.S.C. 119(a)-(d) or (f) or 365(a) or (b) not presented within the time period set forth in 37 CFR 1.55(a)(1) is considered to have been waived. If a claim for foreign priority is presented after the time period set forth in 37 CFR 1.55(a)(1), the claim may be accepted if the claim properly identifies the prior foreign application and is accompanied by a grantable petition to accept an unintentionally delayed claim for priority. See 37 CFR 1.55(c).

4. The following guidelines illustrate the preferred layout for the specification of a utility application. These guidelines are suggested for the applicant's use.

**Arrangement of the Specification**

As provided in 37 CFR 1.77(b), the specification of a utility application should include the following sections in order. Each of the lettered items should appear in upper case, without underlining or bold type, as a section heading. If no text follows the section heading, the phrase "Not Applicable" should follow the section heading:

(a) TITLE OF THE INVENTION.
(b) CROSS-REFERENCE TO RELATED APPLICATIONS.
(c) STATEMENT REGARDING FEDERALLY SPONSORED RESEARCH OR DEVELOPMENT.
(d) THE NAMES OF THE PARTIES TO A JOINT RESEARCH AGREEMENT.
(e) INCORPORATION-BY-REFERENCE OF MATERIAL SUBMITTED ON A COMPACT DISC.
(f) BACKGROUND OF THE INVENTION.

(1) Field of the Invention.
(2) Description of Related Art including information disclosed under 37 CFR 1.97 and 1.98.

(g) BRIEF SUMMARY OF THE INVENTION.
(h) BRIEF DESCRIPTION OF THE SEVERAL VIEWS OF THE DRAWING (S).
(i) DETAILED DESCRIPTION OF THE INVENTION.
(j) CLAIM OR CLAIMS (commencing on a separate sheet).
(k) ABSTRACT OF THE DISCLOSURE (commencing on a separate sheet).
(l) SEQUENCE LISTING (See MPEP § 2424 and 37 CFR 1.821-1.825. A "Sequence Listing" is required on paper if the application discloses a nucleotide or amino acid sequence as defined in 37 CFR 1.821(a) and if the required "Sequence Listing" is not submitted as an electronic document on compact disc).

***Claim Objections***

5. Claims 1, 8, 9, and 10 objected to because of the following informalities:

6. Claims 1, 8, 9, and 10 contain the optional phrase "can be" before describing the claimed invention. This phrase should be changed to indicate that the connection is not optional.

7. A colon should be inserted between the words "comprises" and "a" in Line 5 of Claim 1 to separate the preamble of the claim from the claimed invention.

8. A colon should be inserted between the words "comprises" and "switching" in Line 7 of Claim 8 to designate the limitations of the remote control receiver.

9. In Claim 8, Line 11 states a connection to the "remote control module". It is assumed applicant meant to state a "receiving module" instead of a "remote control module".

10. Items in parentheses in Lines 4-5 of Claim 9 are not considered limitations of the claims.

11. Appropriate correction is required.

***Claim Rejections - 35 USC § 112***

12. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

13. Claim 11 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. Claim 11 describes an additional, activatable clock generator of a higher frequency, which is not shown in any drawings. The description provided in the specification does not provide enough information for one of ordinary skill in the art to make and use the claimed invention.

14. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

15. Claim 9 recites the limitation "the output signal" in the fifth line of Claim 9. There is insufficient antecedent basis for this limitation in the claim. It is unclear if "the output signal" is referring to the output signal of the clock generator or the microcontroller.

***Claim Rejections - 35 USC § 102***

16. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

17. Claims 1, 2, 3, 7, and 8 are rejected under 35 U.S.C. 102(b) as being anticipated by Junichi (Japanese Publication No. JP10-032544).

18. Regarding Claim 1, Junichi anticipates a circuit arrangement for a microcontroller (**Fig. 1, #11**) which is directly or indirectly connected at the input to a module generating an output signal (**Fig. 1, #141**) and can be connected to a clock generator (**Fig. 1, #146**) for the purpose of supply with its operating frequency, characterized in that the circuit arrangement comprises: a switching means (**Fig. 1, #145**) and the microcontroller (**Fig. 1, #11**), in that the signal input of the switching means is connected to the clock generator, the control input of the switching means is directly or indirectly connected to the module generating an output signal, and the output is connected to the microcontroller. The switching means (**Fig. 1, #145**) is shown as the logic AND gate in

Figure 1 of Junichi. The logic gate acts as a switch because it will not pass the clock generator signal unless the clock generator and the other input, which is indirectly connected to the receiving module, carries a logic "1". The output of the switching module (**Fig. 1, #145**) is indirectly connected to the microcontroller through the demodulator (**Fig. 1, #144**) and the bus line (**Fig. 1, #10**) that connects the demodulator to the microcontroller (**Fig. 1, #11**).

19. Regarding Claim 2, Junichi anticipates the circuit arrangement of Claim 1 as stated above. Junichi further anticipates an analyzer (**Fig. 1, #142**) that is connected between the module generating an output signal and the switching means. Junichi discloses the data supervisory circuit (**Fig. 1, #142**), which can be used to detect whether the received signal is useful, or not.

20. Regarding Claim 3, Junichi anticipates the circuit arrangement of Claim 1 as stated above. Junichi further anticipates the output signal of the receiving module (**Fig. 3, #141**) being directly or indirectly applied to the set input of an SR flip-flop (**Fig. 3, #150**), the output of the SR flip-flop (**Fig. 3, DETECT**) connected to the control input of the switching means (**Fig. 3, #145**), and the reset input directly or indirectly connected to an output of the microcontroller. The microcontroller of Junichi shares a bus line (**Fig. 3, #10**) with the demodulator (**Fig. 3, #144**). The microcontroller and demodulator send signals back and forth as shown in Figure 3. Since the reset line of the SR flip-flop receives its signal from part of the demodulator circuit, it can be anticipated that the reset input of the SR flip-flop is indirectly connected to an output of the microcontroller.

21. Regarding Claim 7, Junichi anticipates the circuit arrangement of Claim 1 as stated above. Junichi further clearly anticipates the switching means is an AND gate (**Fig. 3, #145**).

22. Regarding Claim 8, Junichi anticipates a remote control receiver comprising: a receiving module (**Fig. 1, #141**) for receiving an encoded remote control signal, wherein the receiving module is directly or indirectly connected to a microcontroller (**Fig. 1, #11**) for decoding, and the microcontroller can be connected to a clock generator (**Fig. 1, #146**) for the purpose of supply with its operating frequency, characterized in that the remote control receiver comprises: switching means (**Fig. 1, #145**) having a signal input and a control input between the clock generator and the microcontroller, in that the signal input of the switching means is connected to the clock generator, the control input is directly or indirectly connected to the receiving module, and the output is connected to the microcontroller. The switching means shown in Figure 1 of Junichi has a direct signal connection to the clock generator. The control input is indirectly connected to the receiving module through the data supervisory circuit (**Fig. 1, #142**). The output of the switching module (**Fig. 1, #145**) is indirectly connected to the microcontroller through the demodulator (**Fig. 1, #144**) and the bus line (**Fig. 1, #10**) that connects the demodulator to the microcontroller (**Fig. 1, #11**).

23. Claims 9, 10, and 11 are rejected under 35 U.S.C. 102(b) as being anticipated by Watts et al. (European Publication No. EP 0426410).

24. Regarding Claim 9, Watts et al. anticipates a method of operating a microcontroller, which can be connected to a clock generator (**Fig. 3, #540, 550**) for the

purpose of supply with its operating frequency (**Fig. 3, CPU Clock**), characterized in that the program run of the microcontroller determines its switch-off instant (**Col. 13, lines 42-45**), and the output signal brings about the reactivation of the microcontroller (**Col. 14, lines 10-14**). The two oscillators of Watts (**Fig. 3, #540, 550**) form the clock generator that supplies the operating frequency of the microcontroller. The clock generator chooses the operating frequency of the microcontroller based on the instruction received in the sleep input of the flip-flop (**Fig. 3, SPEEP**).

25. Regarding Claim 10, Watts et al. anticipates a remote control receiver comprising a receiving module for receiving an encoded remote control signal, wherein the receiving module is directly or indirectly connected to a microcontroller for decoding and the microcontroller can be connected to a clock generator (**Fig. 3, #540**) for the purpose of supply with its operating frequency, characterized in that the clock generator is connected to the microcontroller when the receiving module detects an input signal and thereupon generates an output signal (**Fig. 3, SPEEP**) for the microcontroller (**Col. 13, lines 42-45**), and that this output signal is additionally applied to a flip-flop which is designed in such a way that it generates a flip flop output signal when it receives the output signal of the receiving module (**Col. 13, lines 45-47**), said flip-flop output signal being applied to the control input of a switching means and thereby through-connecting said switching means and supplying the microcontroller with an operating clock (**Col. 13, lines 47-51**). Watts et al. does not specifically disclose a receiving module, but does disclose a monitor that determines when the microcontroller is ready to sleep (**Col. 13, lines 42-43**). It can be anticipated that this monitor receives some type of control

signal that causes a trigger that the microcontroller is ready to sleep. Therefore, Watts et al. anticipates the receiving module of the remote control receiver.

26. Regarding Claim 11, Watts et al. anticipates the method of Claim 10 as stated above. Watts et al. further anticipates an additional, activatable clock generator of a higher frequency (**Fig. 3, #550**) that is through connected as a clock generator for the microcontroller (**Col. 14, lines 4-10**) after an interrupt signal is sent to the flip-flop. Since the detection of any interrupt within the system of Watts will restore the full clock rate (**Col. 14, lines 10-14**), it can be anticipated that the additional clock generator will have reached its nominal frequency so that it can provide the full clock rate.

***Claim Rejections - 35 USC § 103***

27. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

28. Claim 4 rejected under 35 U.S.C. 103(a) as being unpatentable over Junichi (Japanese Publication JP 10-032544) in view of Watts et al. (European Patent Application EP 0426410). Junichi anticipates the circuit arrangement as claimed in Claim 1. Junichi further anticipates a first JK flip-flop between the module generating the output signal and the switching means. Junichi teaches a SR flip-flop between the module generating the output signal and the switching means (**Fig. 4, #150**). The JK flip-flop can be anticipated because the JK flip-flop augments the performance of the SR

flip-flop by interpreting the S = R = 1 condition as a "flip" command. Since the JK flip-flop can be configured to work as an SR flip-flop, a JK flip-flop can be anticipated from Junichi. However, Junichi fails to anticipate a second JK flip-flop that is arranged between the microcontroller and the K input of the first JK flip-flop. Watts et al. teaches a D flip-flop (**Fig. 3, #500**) that receives an input signal from a monitor (**Col. 13, lines 42-45**). The D flip-flop provides the control signal to the switch between the clock generator and the operating clock of the microcontroller (**Col. 13, lines 47-51**). The monitor receives instruction from the microcontroller, which determines the mode that the microcontroller will operate (**Col. 8, lines 3-13**). Watts et al. can anticipate the JK flip-flop because the JK flip-flop augments the performance of the D flip-flop by setting K equal to the compliment of J. It would have been obvious to someone skilled in the art at the time of the invention to connect the K input of the JK flip-flop anticipated by Junichi to the output of the JK flip-flop anticipated by Watts. The motivation being the use of the two different flip-flops provides a better synchronization method. The JK flip-flop anticipated by Watts would send to the K input of the clock signal of the microcontroller. The JK flip-flop anticipated by Junichi would receive the clock signal of the microcontroller as well as the signal from the received module in the J input. The output of the JK flip-flop would then be provided to the control input of the switching means. By using the JK flip-flops, the switch will only be operational when the clock generator is synchronized with the operating clock of the microcontroller.

29. Claim 5 rejected under 35 U.S.C. 103(a) as being unpatentable over Junichi (Japanese Publication JP 10-032544) in view of Brabrand (US Pub. No. 2002/0163905).

Junichi anticipates the circuit arrangement as claimed in Claim 1 however, Junichi fails to anticipate that a time counter is connected to the clock generator. Brabrand teaches a clock (**Fig. 2, #106**) connected to a counter (**Fig. 1, #113**) in a microcontroller (**Fig. 1, #110**). It would have been obvious to one skilled in the art at the time of the invention to connect a time counter to the clock generator. The motivation being that the time counter will help with synchronization when the switch that connects the clock generator with the microcontroller is activated. Since the operating clock of the microcontroller could already be running, the clock generator must be synchronized with the operating clock of the microcontroller to conserve power.

30. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Junichi (Japanese Publication JP 10-032544) in view of Hanjani (US Patent No. 6,157,265). Junichi anticipates the circuit arrangement as claimed in Claim 1, however Junichi fails to anticipate that the clock generator is an oscillator or a low-frequency quartz generator. Hanjani teaches a clock generation circuit (**Col. 3, lines 32-34**) that contains a multitude of oscillators including a crystal oscillator (**Fig. 2, #210**) and an internal oscillator (**Fig. 2, #216**). The crystal oscillator of Hanjani can be interpreted to be the low-frequency quartz generator. The clock sources are selected to provide the output clock signal (**Col. 3, lines 49-50**). It would have been obvious to one skilled in the art at the time of the invention to combine the clock generation circuit of Hanjani with the clock generator of Junichi. The motivation being the clock generation circuit of Hanjani teaches different types of clock sources that can provide the output clock signal. By using clock generator of Junichi comprising the clock generation circuit of Hanjani, one

could use the type of clock source that would be appropriate for the operating frequency needed for the microcontroller without needing to create different circuits for each frequency.

***Conclusion***

31. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Gayla Futel whose telephone number is 571-270-3008. The examiner can normally be reached on Mon-Thur 7:00 am - 5 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ricky Ngo can be reached on 571-272-3139. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

GF

RICKY Q. NGO
SUPERVISORY PATENT EXAMINER
2/28/07